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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,446	01/12/2004	Theodore Carter Briggs	200313645-1	2130

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,446	BRIGGS ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,10-16 and 18* is/are rejected.

7)☒ Claim(s) *3,4,7-9 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This Office Action is in response to applicant's communication filed July 6, 2006 in response to the PTO Office Action mailed April 6, 2006. The applicant's remarks were considered with the results that follow.

2. In response to the last Office Action, no claims have been cancelled, amended, or added. Claims 1-18 remain pending in this application.

3. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 12 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by House (US Patent No. 4,796,232).

For claim 12, House discloses a method for data transfer between a memory controller and a system memory bus connected to a system memory in a computing system comprising:

interposing a buffer between said system memory bus and the memory controller (col. 5, lines 10-16; fig. 1, items 60-63, 80-83, 40-48; col. 4, lines 6-8);

providing to said buffer memory interface addresses and memory interface control commands to facilitate said buffer's read and write operations from and to said system memory (fig. 1, items 40-48, 50-53, 70-73);

addressing said system memory through said buffer to accomplish read and write operations between the system memory and the memory controller (fig. 1, items 40-48, 50-53, 70-73);

decoding in said buffer the memory interface control commands (col. 4, lines 6-8);

temporarily storing data read and write memory data in the buffer during data transfer between the system memory and the buffer (col. 5, lines 10-16); and

transferring read and write memory data between said memory controller and said buffer during read and write operations (col. 5, lines 10-16).

For claim 15, House discloses the invention as per rejection of claim 12 above.

House further discloses controlling read and write operations to said system memory with the decoded memory interface control commands originating in the memory controller and decoded in the buffer (a request by a pcoessor is applied to terminal of gate array and an appropriate address is applied to an address buffer while

data is received through a data buffer, col. 6, lines 53-64; a write control is coupled to terminal of gate array by a processor and an address is coupled to address buffer while the desired data to be stored is applied to data buffer, col. 6, lines 65-68, col. 7, lines 1-3; fig. 1).

For claim 16, House discloses the invention as per rejection of claim 12 above. House further discloses fanning memory address information received in the buffer from the controller to the system memory through a data address control bus connecting the buffer to the system memory bus (House: fig. 1, port_A and port_B address buses).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-6, 10-11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Platko et al (US Patent No. 6,363,444) in view of House (US Patent No. 4,796,232).

For claim 1, Platko discloses a memory control apparatus in a computing system comprising:

a memory controller and a buffer (a memory controller controls the SRAM and the memory bus, col. 3, lines 44-45; where all packets either transmitted or received are temporarily buffered in the SRAM, col. 4, lines 3-4);

said memory controller and buffer being connected by a bidirectional data bus and a control interface (fig. 1, items 20, 22, 46); and

said buffer being connected to a random-access memory bus for read and write operations (fig. 1, items 20, 22, 46).

Platko fails to disclose the remaining claim limitations.

House helps disclose said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller (data buffers... include a data bus input, a memory data bus output and a control signal input, col. 5, lines 10-16; fig. 1, items 60-63, 80-83, 40-48; a dual port memory controller which includes a dedicated logic array coupled to an arbitrator system, col. 4, lines 6-8);

and a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory (a memory array includes... individual memory banks, all of which are commonly coupled to a memory data bus terminal, where the memory is constructed in accordance with conventional dynamic RAM memories, col. 4, lines 47-55; fig. 1, items 11-16).

Platko and House are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. House suggests that it would have been desirable to incorporate buffer data storage areas and a data access and control bus connected between the buffer and system memory into the system of Platko because this would aid in the control of the transfer of information to and from

memory (col. 5, lines 36-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Platko as suggested by House to incorporate the feature as claimed.

For claim 5, Platko and House disclose the invention as per rejection of claim 1 above.

Platko and House further disclose the control interface between the memory controller and buffer comprises a memory interface address bus for transferring memory addresses from the memory controller to the buffer (House: fig. 1, port_A and port_B address buses).

For claim 6, Platko and House disclose the invention as per rejection of claim 1 above.

Platko and House further disclose the control interface between the controller and buffer comprises a memory interface control bus for transferring memory control commands from the controller to the buffer (House: fig. 1, port control A, port control B).

For claim 10, Platko and House disclose the invention as per rejection of claim 1 above.

Platko and House further disclose the buffer comprises control logic for decoding memory interface control commands (House: col. 4, lines 6-8).

For claim 11, Platko and House disclose the invention as per rejection of claim 1 above.

Platko and House further disclose the buffer comprises multiple data and control interfaces to system memory, one to interface with each independent portion of system memory (fig. 1).

For claim 18, Platko discloses a memory control apparatus in a computing system comprising:

a memory controller and a means for buffering data between said controller and system memory (col. 3, lines 44-45; col. 4, lines 3-4); and

said memory controller and buffer means being connected by a bidirectional data bus and a control interface (fig. 1, items 20, 22, 46).

Platko fails to disclose the remaining claim limitations.

House helps disclose said buffer means being connected to multiple random-access memory busses for read and write operations (fig. 1, items 11-33, 60-63, 80-83, 40-48);

said buffer means comprising means for temporarily storing data exchanged between the memory controller and system memory, said buffer means further comprising logical circuits to decode memory interface control commands from said memory controller (col. 5, lines 10-16; fig. 1, items 60-63, 80-83, 40-48; col. 4, lines 6-8);

and a data access and control bus connected between the buffer and the multiple random-access memory busses to control read and write operations from and to system memory (fig. 1, items 11-33, 60-63, 80-83, 40-48).

Platko and House are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. House suggests that it would have been desirable to incorporate buffer data storage areas and a data access and control bus connected between the buffer and system memory into the system of Platko because this would aid in the control of the transfer of information to and from memory (col. 5, lines 36-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Platko as suggested by House to incorporate the feature as claimed.

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over House (US Patent No. 4,796,232) in view of Fortuna et al (US Patent No. 6,546,464).

For claim 13, House discloses the invention as per rejection of claim 12 above.

House fails to disclose interposing a second buffer between the controller and system memory serving as a tag buffer.

Fortuna helps disclose a processor module including system memory, direct memory access device(s), memory controller, processor(s) with associated cache(s) and tag buffer (col. 4, lines 51-55; fig. 1).

House and Fortuna are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Fortuna suggests that it would have been desirable to incorporate a tag buffer system into the dual-buffered system of House because this would help increase data rates while maintaining system coherency (col. 2, lines 13-16). Therefore, it would have been obvious to a person of

ordinary skill in the art at the time the invention was made to modify House as suggested by Fortuna to incorporate the feature as claimed.

For claim 14, House and Fortuna disclose the invention as per rejection of claim 13 above.

House and Fortuna further disclose updating memory tag information through a tag interface control bus between the memory controller and the tag buffer (Fortuna: a separate tag buffer which maintains the tag entries for the system memory, col. 5, lines 45-47; fig. 1, items 108, 112).

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Platko et al (US Patent No. 6,363,444) in view of House (US Patent No. 4,796,232) and further in view of Fortuna et al (US Patent No. 6,546,464).

For claim 2, Platko and House disclose the invention as per rejection of claim 1 above.

Platko and House fail to disclose a second buffer serving as a tag buffer, said second buffer being connected to said random-access memory bus for read and write operations;

said second buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

a data access and control bus connected between the tag buffer and the system memory to control read and write operations from and to system memory.

Fortuna helps disclose a processor module including system memory, direct memory access device(s), memory controller, processor(s) with associated cache(s) and tag buffer (col. 4, lines 51-55; fig. 1).

Platko, House and Fortuna are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Fortuna suggests that it would have been desirable to incorporate a tag buffer system into the dual-buffered system of Platko and House because this would help increase data rates while maintaining system coherency (col. 2, lines 13-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Platko and House as suggested by Fortuna to incorporate the feature as claimed.

Allowable Subject Matter

10. Claims 3-4, 7-9 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 indicates allowable subject matter because of prior art found or of record or any combination thereof describes "a tag control input signal designating said second buffer as the tag buffer".

Claim 4 indicates allowable subject matter based on its dependency on claim 3 and containing additionable allowable features therein.

Claim 7 indicates allowable subject matter because of prior art found or of record or any combination thereof describes the buffer comprises "a read data queue".

Claim 8 indicates allowable subject matter because of prior art found or of record or any combination thereof describes the buffer comprises "a write data queue".

Claim 9 indicates allowable subject matter because of prior art found or of record or any combination thereof describes the buffer comprises "a tag data queue".

Claim 17 indicates allowable subject matter because of prior art found or of record or any combination thereof describes "interleaving read and write operations in sequences of memory operations between the controller and multiple independent portions of system memory through the buffer".

Contact Information

11. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions

regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

1-25-07

STEPHEN C. ELMORE
PRIMARY EXAMINER